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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,461	03/07/2002	Masataka Ito	00862.022541	8794

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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,461	ITO, MASATAKA	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: On pages 7 and 8 lines 24 and 4 respectively under the DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS, the reference number 7 pertaining to a wafer boat is not shown in the drawings. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Response to Arguments

2. Applicant's arguments with respect to claims 1-8 and 10-17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8 and 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Ishii et al US Patent 5,820,683 in view of Pein US Patent 5,378,912.

4. Ishii discloses the semiconductor method substantially as claimed. See **FIGS. 1-9** where Ishii teaches an annealing method of annealing an SOI substrate in a reducing atmosphere, comprising the step of:

holding the substrate by a holding portion **36** having a surface formed from silicon and annealing the SOI substrate, wherein the holding portion is a member having a silicon film thereon or a member formed from single-crystal silicon or polysilicon.

However Ishii fails the step of holding the SOI substrate. See **col. 1 line 10-23,** where Ishii teaches holding the SOI substrate. In view of Ishii it would have been obvious to one of ordinary skill in the art to incorporate an SOI substrate because the manufacturing process of a semiconductor device, such as formation of an oxide film, diffusion of impurities and film forming, various kinds of heat processing are performed on semiconductor wafers.

5. Pertaining to claim 2, Ishii teaches the method according to claim 1, wherein the annealing is executed at a temperature lower than a melting point of single-crystal silicon.

6. Pertaining to claim 3, Ishii teaches the method according to claim 1, wherein the annealing is executed at a temperature not less than 775°C.

7. Pertaining to claim 4, Ishii teaches the method according to claim 1, wherein the annealing is executed at a temperature not less than 966°C.

8. Pertaining to claim 5, Ishii teaches the method according to claim 1, wherein the annealing is executed at a temperature not less than 993°C.

9. Pertaining to claim 6, Ishii teaches an SOI substrate manufactured using an annealing method of claim 1.

10. Pertaining to claim 8, Ishii teaches a semiconductor device manufacturing method, comprising the steps of:

annealing an SOI substrate using an annealing method of claim l; and

forming an active region for a transistor in a nonporous semiconductor layer of the SOI substrate.

11. Pertaining to claim 10, Ishii teaches an annealing method of annealing an SOI substrate in a reducing atmosphere, comprising the step of:

holding the substrate by a holding portion which contains no silicon carbide formed by sintering and has a surface formed from silicon carbide deposited by CVD and annealing the SOI substrate.

However Ishii fails the step of holding the SOI substrate. See **col. 1 line 10-23,** where Ishii teaches holding the SOI substrate. In view of Ishii it would have been obvious to one of ordinary skill in the art to incorporate an SOI substrate because the manufacturing process of a semiconductor device, such as formation of an oxide film, diffusion of impurities and film forming, various kinds of heat processing are performed on semiconductor wafers.

12. Pertaining to claim 11, Ishii teaches the method according to claim 10, wherein the annealing is executed at a temperature lower than a melting point of single-crystal silicon.

13. Pertaining to claim 12, Ishii teaches the method according to claim 10, wherein the annealing is executed at a temperature not less than 775°C.

14. Pertaining to claim 13, Ishii teaches the method according to claim 10,wherein the annealing is executed at a temperature-not less than 966°C.

15. Pertaining to claim 14, Ishii teaches the method according to claim 10, wherein the annealing is executed at a temperature not less than 993°C.

16. Pertaining to claim 15, Ishii teaches an SOI substrate manufactured using an annealing method of claim 10.

17. Pertaining to claims 7 and 16, Ishii fails the substrate according to claim 6, wherein an HF defect density is not more than 0.05 defects /cm^2. Given the teachings of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. *See In re Aller, Lancey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575,1578,16 USPQ2d 1934, 1934 (Fed. Cir. 1990).

18. Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)

19. Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

20. An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

21. Pertaining to claim 17, Ishii teaches a semiconductor device manufacturing method, comprising the steps of:

22. annealing an substrate using an annealing method of claim 10.

However Ishii fails the step of holding the SOI substrate. See **col. 1 lines 10-23,** where Ishii teaches holding the SOI substrate. In view of Ishii it would have been obvious to one of ordinary skill in the art to incorporate an SOI substrate because the manufacturing process of a semiconductor device, such as formation of an oxide film, diffusion of impurities and film forming, various kinds of heat processing are performed on semiconductor wafers.

23. In addition, Ishii fails the step of forming an active region for a transistor in a nonporous semiconductor layer of the SOI substrate. See **FIG. 3** where Pein teaches step of forming an active region for a transistor in a nonporous semiconductor layer of the SOI substrate. In view of Pein it would have been obvious to one of ordinary skill in the art to incorporate Pein into Ishii because the semiconductor material can be made from silicon carbide (SiC). (See **col. 4 lines 5-40**)

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 703-308-5871. The examiner can normally be reached on Monday-Friday 7:30am -5:30pm.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Nebling can be reached on 703-308-3325. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

26. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Stanetta Isaac
Patent Examiner
November 7, 2003